8-bit addressable latch   74HC/HCT259

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The "259" are multifunctional devices capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available.

The "259" also incorporates an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as, an active LOW enable input ($\overline{LE}$).

The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	D to Q_n		18	20	ns
	A_n, $\overline{LE}$ to Q_n		17	20	ns
t_{PHL}	$\overline{MR}$ to Q_n		15	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

    $P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \Sigma (C_L \times V_{CC}{}^2 \times f_o)$ where:

    f_i = input frequency in MHz

    f_o = output frequency in MHz

    $\Sigma (C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs

    C_L = output load capacitance in pF

    V_{CC} = supply voltage in V

2. For HC   the condition is V_I = GND to V_{CC}
    For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
$\overline{LE}$	1.50
D	1.20
$\overline{MR}$	0.75

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25			−40 TO +85		−40 TO +125		UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D to Q_n		23	39		49		59	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay A_n to Q_n		25	41		51		62	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n		22	38		48		57	ns	4.5	Fig.6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		23	39		49		59	ns	4.5	Fig.9
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t_W	$\overline{LE}$ pulse width LOW	19	11		24		29		ns	4.5	Fig.6
t_W	$\overline{MR}$ pulse width LOW	18	10		23		27		ns	4.5	Fig.9
t_{su}	set-up time D to $\overline{LE}$	17	10		21		26		ns	4.5	Fig.10
t_{su}	set-up time A_n to $\overline{LE}$	17	10		21		26		ns	4.5	Fig.11
t_h	hold time D to $\overline{LE}$	0	−8		0		0		ns	4.5	Fig.10
t_h	hold time A_n to $\overline{LE}$	0	−4		0		0		ns	4.5	Fig.11